AMENDMENTS TO THE CLAIMS

(IN FORMAT COMPLIANT WITH THE REVISED 37 CFR 1.121)

Please cancel claims 5 and 21 without prejudice.

1. (CURRENTLY AMENDED) A digital cross connect comprising:

plural switching stages, each stage having plural switches receiving plural frames of time multiplexed input data and switching the data in time and space; and

configuration storage at each switch storing a time/space configuration for the switch, all switches switching configuration to the stored time/space configuration in frame synchronization at the start of synchronized data frames by synchronizing switches of successive stages to a configuration select signal propagated from at least one switch of an input stage, wherein configuration switching is initiated by a prepare-to-switch signal propagated from a master switch to all switches of an output stage and the input stage, the at least one switch of the input stage then propagating the configuration select signal.

2. (PREVIOUSLY PRESENTED) The digital cross connect as claimed in claim 1, wherein the configuration select signal is embedded within a frame of data.

3. (PREVIOUSLY PRESENTED) The digital cross connect as claimed in claim 2, wherein the configuration select signal is embedded in an A1 byte of a SONET frame.

4. (PREVIOUSLY PRESENTED) The digital cross connect as claimed in claim 3, wherein the configuration select signal is embedded in the fourth A1 byte of an STS-48 frame.

5. (CANCELED)

6. (CURRENTLY AMENDED) The digital cross connect as claimed in claim ~~5~~ 1, wherein the prepare-to-switch signal is embedded within a frame of data.

7. (PREVIOUSLY PRESENTED) The digital cross connect as claimed in claim 6, wherein the prepare-to-switch signal is embedded in an A1 byte of a SONET frame.

8. (PREVIOUSLY PRESENTED) The digital cross connect as claimed in claim 7, wherein the prepare-to-switch signal is embedded in the second and third bytes of an STS-48 frame.

9. (CURRENTLY AMENDED) The digital cross connect as claimed in claim ~~5~~ 1, wherein switches of the first and last stages are on common chips.

10. (PREVIOUSLY PRESENTED) The digital cross connect as claimed in claim 9, wherein the common chips of the first and last stages support respective framing time bases for the first and last stages.

11. (PREVIOUSLY PRESENTED) The digital cross connect as claimed in claim 9, wherein connections from the first stage expand in space from input connections, and connections to the last stage concentrate in space to output connections.

12. (PREVIOUSLY PRESENTED) The digital cross connect as claimed in claim 11, wherein chips of a common design support the switches of all stages.

13. (CURRENTLY AMENDED) The digital cross connect as claimed in claim ~~5~~ 1, wherein the prepare-to-switch signal from the master switch is in a signal which is qualified to distinguish the signal from the master switch from signals from other switches.

14. (PREVIOUSLY PRESENTED) The digital cross connect as claimed in claim 13, wherein the qualifier and the configuration data are embedded in A1 bytes of a SONET frame.

15. (CURRENTLY AMENDED) The digital cross connect as claimed in claim ~~5~~ 1, wherein the master switch is in a middle stage.

16. (PREVIOUSLY PRESENTED) The digital cross connect as claimed in claim 1, wherein each switch comprises a time slot interchanger associated with each input and output port thereof and a space switch.

17. (CURRENTLY AMENDED) A method of cross connecting digital data comprising:

providing plural switching stages, each stage having plural switches receiving plural frames of time multiplexed input data and switching the data in time and in space;

providing configuration storage at each switch to store a time/space configuration for the switch;

propagating a configuration select signal from at least one input switch of an input stage to successive stages; and

switching configuration of the switches to the stored time/space configurations in frame synchronization at the start of synchronized data frames by synchronizing switches of the successive stages to the configuration select signal, wherein configuration switching is initiated by a prepare-to-switch signal propagated from a master switch to all switches of an output stage and the input stage, the at least one switch of the input stage then propagating the configuration select signal.

18. (PREVIOUSLY PRESENTED) The method as claimed in claim 17, wherein the configuration select signal is embedded within a frame of data.

19. (PREVIOUSLY PRESENTED) The method as claimed in claim 18, wherein the configuration select signal is embedded in an A1 byte of a SONET frame.

20. (PREVIOUSLY PRESENTED) The method as claimed in claim 19, wherein the configuration select signal is embedded in the fourth A1 byte of an STS-48 frame.

21. (CANCELED)

22. (CURRENTLY AMENDED) The method as claimed in claim ~~21~~ 17, wherein the prepare-to-switch signal is embedded within a frame of data.

23. (PREVIOUSLY PRESENTED) The method as claimed in claim 22, wherein the prepare-to-switch signal is embedded in an A1 byte of a SONET frame.

24. (PREVIOUSLY PRESENTED) The method as claimed in claim 23, wherein the prepare-to-switch signal is embedded in the second and third bytes of an STS-48 frame.

25. (CURRENTLY AMENDED) The method as claimed in claim ~~21~~ 17, wherein switches of the first and last stages are on common chips.

26. (PREVIOUSLY PRESENTED) The method as claimed in claim 25, further comprising switching the data of the first and last stages in synchronization with respective framing time bases for the first and last stages.

27. (PREVIOUSLY PRESENTED) The method as claimed in claim 25, wherein the frames from the first stage expand in space from input connections, and frames to the last stage concentrate in space to output connections.

28. (PREVIOUSLY PRESENTED) The method as claimed in claim 27, wherein chips of a common design support the switches of all stages.

29. (CURRENTLY AMENDED) The method as claimed in claim ~~21~~ 17, wherein the prepare-to-switch signal from the master switch is in a signal which is qualified to distinguish the master signal from signals from other switches.

30. (PREVIOUSLY PRESENTED) The method as claimed in claim 29, wherein the qualifier and the configuration data are embedded in A1 bytes of a SONET frame.

31. (CURRENTLY AMENDED) The method as claimed in claim 21, wherein ~~the~~ a master switch is in a middle stage.

32. (PREVIOUSLY PRESENTED) The method as claimed in claim 17, wherein each switch comprises a time slot interchanger associated with each input and output port thereof and a space switch.

33. (CURRENTLY AMENDED) A digital cross connect comprising:

plural switching stages, each stage having plural switching means for receiving plural frames of time multiplexed input data and switching the data in time and space;

configuration storage means at each switch for storing a time/space configuration for the switch; and

means for switching configuration of the switches to the stored time/space configuration in synchronization with a configuration select signal propagated from at least one input switching means of an input stage, wherein (i) configuration switching is initiated by a prepare-to-switch signal propagated from a master switch to all switches of an output stage and the input stage and (ii) the at least one input switching means of the input stage then propagating the configuration select signal.

34. (CURRENTLY AMENDED) A digital cross connect comprising:

plural switching stages, each stage having plural switches, each comprising a time slot interchanger associated with each input and output port thereof and a space switch, each switch

receiving plural frames of time multiplexed input data and switching the data in time and space; and

configuration storage at each switch storing a time/space configuration for the switch, all switches switching configuration to the stored time/space configuration in frame synchronization at the start of synchronized data frames, wherein (i) configuration switching is initiated by a prepare-to-switch signal propagated from a master switch to all switches of an output stage and (ii) at least one switch then propagating the configuration select signal.

35. (CURRENTLY AMENDED) A method of cross connecting digital data comprising:

providing plural switching stages, each stage having plural switches, each comprising a time slot interchanger associated with each input and output port thereof and a space switch, each switch receiving plural frames of time multiplexed input data and switching the data in time and in space;

providing configuration storage at each switch to store a time/space configuration for the switch; and

switching configuration of the switches to the stored time/space configurations in frame synchronization at the start of synchronized data frames by synchronizing switches of the successive stages to the configuration select signal, wherein (i) configuration switching is initiated by a prepare-to-switch signal propagated from a master switch to all switches of an output and

(ii) at least one switch then propagating the configuration select signal.

36. (CURRENTLY AMENDED) A digital cross connect comprising:

plural switching stages, each stage having plural switching means, each comprising a time slot interchanger associated with each input and output port thereof and a space switch, for receiving plural frames of time multiplexed input data and switching the data in time and space;

configuration storage means at each switch for storing a time/space configuration for the switch; and

means for switching configuration of the switches to the stored time/space configuration in frame synchronization at the start of synchronized data frames, wherein (i) configuration switching is initiated by a prepare-to-switch signal propagated from a master switch to all switches of an output stage and (ii) at least one switch then propagating the configuration select signal.

37. (ORIGINAL) A digital cross connect comprising plural switching stages, each stage having plural switches on plural chips receiving plural frames of time multiplexed input data and switching the data in time and space, switches of different stages being on common chips supporting respective framing time bases for the different stages.

38. (PREVIOUSLY PRESENTED) The digital cross connect as claimed in claim 37, wherein connections from a first stage expand in space from input connections and connections to a second stage concentrate in space to output connections.

39. (PREVIOUSLY PRESENTED) The digital cross connect as claimed in claim 37, wherein the different stages are first and final stages of the plural switching stages.

40. (PREVIOUSLY PRESENTED) The digital cross connect as claimed in claim 39, wherein connections from the first stage expand in space from input connections, and connections to the final stage concentrate in space to output connections.

41. (ORIGINAL) A switch circuit on an integrated circuit chip comprising:

switch circuitry receiving plural frames of time multiplexed input data and switching the data in time and space;

a first frame counter to which a first portion of the plural frames of time multiplexed input data is synchronized; and

a second frame counter to which a second portion of the plural frames of time multiplexed input data is synchronized.

42. (PREVIOUSLY PRESENTED) The switch circuit as claimed in claim 41, wherein connections expand in space from input

connections to the first portion, and connections concentrate in space to output connections of the second portion.

43. (PREVIOUSLY PRESENTED) The switch circuit as claimed in claim 41, wherein the switch circuitry responds to a prepare-to-switch signal received with the second portion to initiate a configuration select signal propagated with the first portion.

44. (PREVIOUSLY PRESENTED) The switch circuit as claimed in claim 43, wherein the configuration select signal is embedded within a frame of data.

45. (PREVIOUSLY PRESENTED) The switch circuit as claimed in claim 44, wherein the configuration select signal is embedded in an A1 byte of a SONET frame.

46. (PREVIOUSLY PRESENTED) The switch circuit as claimed in claim 45, wherein the configuration select signal is embedded in the fourth A1 byte of an STS-48 frame.

47. (PREVIOUSLY PRESENTED) The switch circuit as claimed in claim 44, wherein the prepare-to-switch signal is embedded within a frame of data.

48. (PREVIOUSLY PRESENTED) The switch circuit as claimed in claim 47, wherein the configuration select signal and the

prepare-to-switch signal are embedded within A1 bytes of a SONET frame.

49. (PREVIOUSLY PRESENTED) The switch circuit as claimed in claim 43, wherein the prepare-to-switch signal is embedded within a frame of data.

50. (PREVIOUSLY PRESENTED) The switch circuit as claimed in claim 49, wherein the prepare-to-switch signal is embedded in an A1 byte of a SONET frame.

51. (PREVIOUSLY PRESENTED) The switch circuit as claimed in claim 50, wherein the prepare-to-switch signal is embedded in the second and third bytes of an STS-48 frame.

52. (PREVIOUSLY PRESENTED) The switch circuit as claimed in claim 41, wherein input frames to and output frames from the switch circuitry are programmably assignable to the first and second portions.